Configurable hardware A new paradigm for computation:

* If there’s a delay for routing, can’t we group the most used functions in better locations to reduce those delays?
* At this step in 89’ the advantage was more computation power or more agility configuring the systems?

Garp architecture and C compiler:

* I couldn’t understand if they put the chip inside the system as a design, because they state, the GARP chip does not exist as real silicon.
* Page 3, in the last paragraph, one of the challenges was that each instruction should be parallelized, and all of the code in general should be parallel. I would expected to see how it reduces the speed prior and after the Garp, it is very reasonable that high percentage of the compilation improvement will relate to that.

The Stratix™ 10 Highly Pipelined FPGA Architecture:

* If FPGA’s has around dozen clocks, how are they synchronized with each other and with the rest of the system?
* It’s clear that this logical pipelined architecture has 2X performance, is it generalized and if so, why it’s not being used as a concept in FPGA’s?